LOW POWER DESIGN OF DIGITAL SYSTEMS USING ENERGY RECOVERY CLOCKING AND CLOCK GATING

A thesis work submitted to the faculty of
San Francisco State University
In partial fulfillment of the
requirements for
The degree

Master of Science
In
Engineering

by

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San Francisco, California

October, 2007

CERTIFICATION OF APPROVAL

I certify that I have read Low Power Design of Digital Systems Using Energy Recovery Clocking and Clock Gating by Vishwanadh Tirumalashetty, and that in my opinion this work meets the criteria for approving a thesis submitted in partial fulfillment of the requirements for the degree: Master of Science in Engineering at San Francisco State University

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2007

Energy recovery clocking has been demonstrated as an effective method for reducing the clock power. However, in this method the conventional square wave clock signal is replaced by a sinusoidal clock generated by a resonant circuit. Such a modification in clock signal prevents application of existing clock gating solutions. In this paper, we propose clock gating solutions for energy recovery clocking by gating the flip-flops or the clock generator. According to simulations results in 0.25um CMOS technology, applying our clock gating to the energy recovery clocked flip-flops reduces their power by 1000X in the idle mode with negligible power and delay overhead in the active mode. Applying the proposed clock gating technique to a system of 1000 flip-flops with idle mode probability and data switching activity of 50%, reduces the total power by 47%. We also propose negative edge triggering solution for the energy recovery clocked flip-flops.

I certify that the Abstract is a correct representation of the content of this thesis.

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Chair, Thesis Committee Date

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Hamid Mahmoodi for his invaluable advice and support towards the completion of my thesis. I would like to thank my engineering department for providing me the resources required for completing my project. I would like to thank Dr. Ying Chen for her timely feedbacks. I would like to thank my family and friends for their support.

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1. Introduction

Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. Traditionally, the demand for high performance was addressed by increasing clock frequencies with the help of technology scaling. However, in deep sub-micron generations, the increasing trend in clock frequency has slowed down and instead higher performance is obtained by increasing parallelism at the architectural level. A very clear example of this trend is the recent move towards multi-core architectures for processors [1]. With the continuing increase in the complexity of high-performance VLSI system-on-chip (SOC) designs, the resulting increase in power consumption has become the major obstacle to the realization of high-performance designs. Such increase in the complexity of synchronous SOC systems, increases the complexity of the clock network and hence increases the clock power even if the clock frequency may not scale anymore. Hence, the major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. In the Xeon Dual-core processor, a significant portion of the total chip power is due to the clock distribution network [1]. Thus, innovative clocking techniques for decreasing the power consumption of the clock networks are required for future high performance and low power designs.

Energy recovery is a technique originally developed for low-power digital circuits [2]. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their

capacitors by using an AC-type (oscillating) supply voltage [2]. In this paper, we apply energy recovery techniques to the clock network since the clock signal is typically the most capacitive signal in a chip. The proposed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal. The rest of the system is implemented using standard circuit styles with a constant supply voltage. However, for this technique to work effectively there is a need for energy recovery clocked flip-flops that can operate with a sinusoidal clock. A pass-gate energy recovery clocked flip-flop has been proposed in [3] that works with a four-phase sinusoidal clock. The main disadvantage of the pass-gate energy recovery clocked flip-flop is that its delay takes a major fraction of the total cycle time; therefore, the time allowed for combinational logic evaluation is significantly reduced. In addition, it requires four phases of the clock, adding considerable overhead to clock generation and routing. In this paper, we propose four high-performance and low-power energy recovery clocked flip-flops that operate with a single-phase sinusoidal clock. The proposed flip-flops exhibit significant reduction in delay, power, and area as compared to the four-phase pass-gate energy recovery clocked flip-flop.

Clock gating is another popular technique for reducing clock power [10]. Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the clock network due to resistances of the clock network and the energy loss in the oscillator itself due to non-adiabatic switching. Hence, it is still desirable to apply clock gating to the energy recovery clock for further reducing

the clock power during idle periods. The existing clock gating solutions are based on masking the local clock signal using masking logic gates (NAND/NOR) [10]. These methods of clock gating do not work for energy recovery clocking. This is because insertion of masking logic gates eliminates energy recovery from the remaining capacitances in downstream fan-out. To the best of our knowledge there have not been any clock gating solutions proposed for the energy recovery clocking.

In this research, we propose clock gating solutions for the energy recover clock. We modify the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip-flops. Applying the proposed clock gating technique to the flip-flops reduces their power by a substantial amount (1000X) during the sleep mode. Moreover, the added feature has negligible power and delay overhead when flip-flops are in the active mode.

In most synchronous systems it is required to use both positive and negative edge triggered flip-flops. Obtaining negative edge triggering in conventional square wave clocked flip-flops is easily done by inverting the input clock signal using an inverter logic gate. This approach however is not applicable to the energy recovery clocked flip-flops since insertion of an inverter logic gate in the path of an energy recovery clock changes the shape of the clock and eliminates the energy recovery property. To the best of our knowledge there have not been any negative edge triggered energy recovery clocked flip-flops proposed in the literature. In this research, we propose a class of negative edge triggered energy recovery clocked flip-flops.

The remainder of this thesis is organized as follows. Section 2 includes introduction to the energy recovery clock, the impact of Process Voltage-Temperature (PVT) variations on the energy recovery clock and the application of clock gating to the energy recovery clock. In section 3, the conventional four-phase pass-gate energy recovery clocked flip-flop is reviewed, the energy recovery clocked flip-flops are described, the clock gating approaches are proposed for energy recovery clocked flip-flops, extensive simulation results of individual flip-flops and their comparisons are presented.. In Section 4, includes a summary of all the results obtained. In Section 5, negative edge triggered energy recovery clocked flip-flops are presented. Section 6 includes the comparison of different clock gating approaches. Finally, the conclusion of the thesis appears in Section 8.

2. Energy Recovery Clock

The basic principle of energy recovery is to recycle the energy stored in the capacitors by using the LC network. This principle of energy recovery is not applicable to the square wave clock generators. In order to make energy recovery possible we require sinusoidal clock signals. The proposed energy recovery clock generator is a LC Oscillator that generates sinusoidal clock signals. We generate square wave clock signals using the ring oscillator shown in Figure 1(b). It is a non energy recovering network as the energy stored in the load capacitor is discharged in each cycle of the clock.

The energy recovery clock generator is a single-phase resonant clock generator as shown in Fig. 1(a) recycles the energy from the capacitance in each cycle of the clock. Transistor M1 receives a reference pulse to pull-down the clock signal to ground when the clock reaches its minimum; thereby maintaining the oscillation of the resonant circuit. This transistor is a fairly large transistor, and therefore, driven by a chain of progressively sized inverters. The natural oscillation frequency of this resonant clock driver is determined by:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

where C is the total capacitance connected to the clock-tree including parasitic capacitances of the clock-tree and gate capacitances associated with clock inputs of all flip-flops. In order to have an efficient clock generator, it is important that the frequency of the REF signal be the same as the natural oscillation frequency of the resonant circuit.

In order to find the value of *C*, first with a given *L* and with the REF signal at zero, the whole system, including the flip-flops, is simulated. The clock signal shows a decaying oscillating waveform settling down to $V_{dd}/2$. From this waveform the natural decaying frequency is measured, and then by using Equation (1), the value of *C* is calculated. For the system with each proposed flip-flop, this experiment is carried out to determine the value of *C*. Having the value of *C*, the value of *L* for the frequency of 200MHz can again be determined from the Equation (1).The system consisting of the energy recovery clock generator, clock-tree, and flip-flops was simulated at the frequency of 200MHz (for all the proposed energy recovery clocked flip-flops) with different data switching activities.

In order to demonstrate the feasibility of energy recovery clocking, we integrated 1024 energy recovery clocked flip-flops distributed across an area of 4mm × 4mm and clocked them by a single-phase sinusoidal clock through an H-tree clocking network. The flips-flops were grouped into registers of 32 flip-flops, and the registers were evenly spaced in this area. A common data input was used for all flip-flops to easily control the data switching activity of the system. The clock was distributed using an H-tree network on the metal-5 layer, which has the smallest parasitic capacitance to the substrate. The width of the clock-tree interconnects was selected to be the maximum (35μm in our 0.25μm process) to minimize parasitic resistances. Wider wires also minimize clock skew [11]. The study in [11] shows that with proper sizing and spacing of clock wires, the clock skew of a resonant clock can be comparable or even better than a square wave clock network. A lumped ∏-type RC model for each interconnect of the clock-tree was

extracted and then connected together to make a distributed RC model of the clock-tree, as shown in Fig. 2. The energy recovery clock generator drives the source node of the clock-tree (node CLK in Fig. 2), and each final node of the clock-tree (CLK1 to CLK16) is connected to two 32-bit flip-flop registers [12].

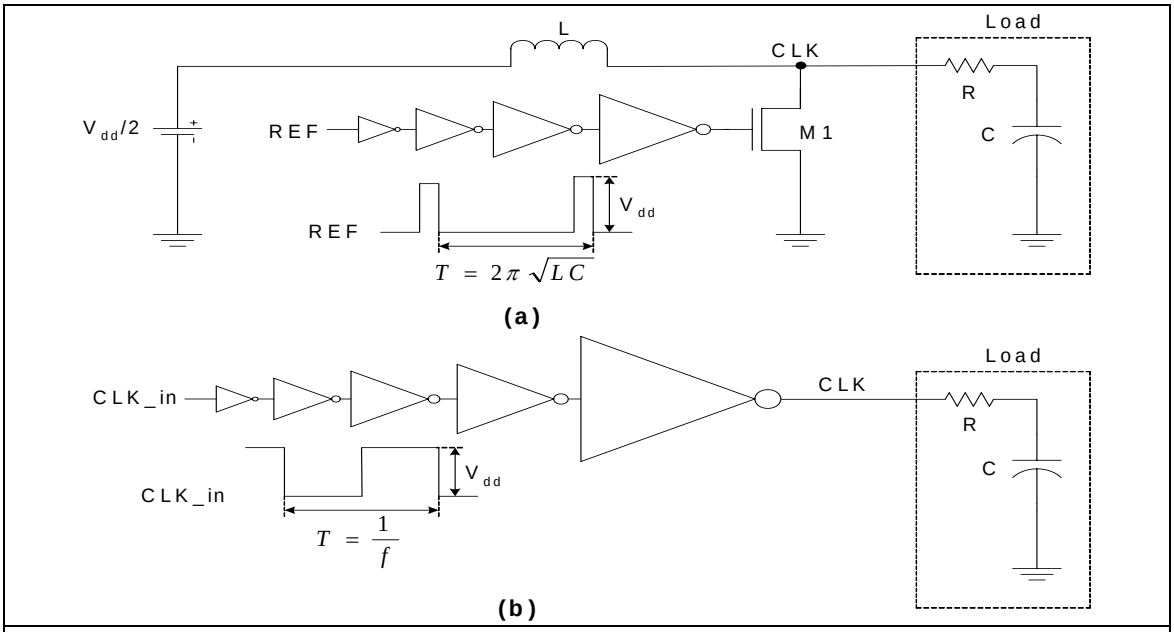

Fig 1: (a) Resonant energy recovery clock generator (b) Non-energy recovery clock driver

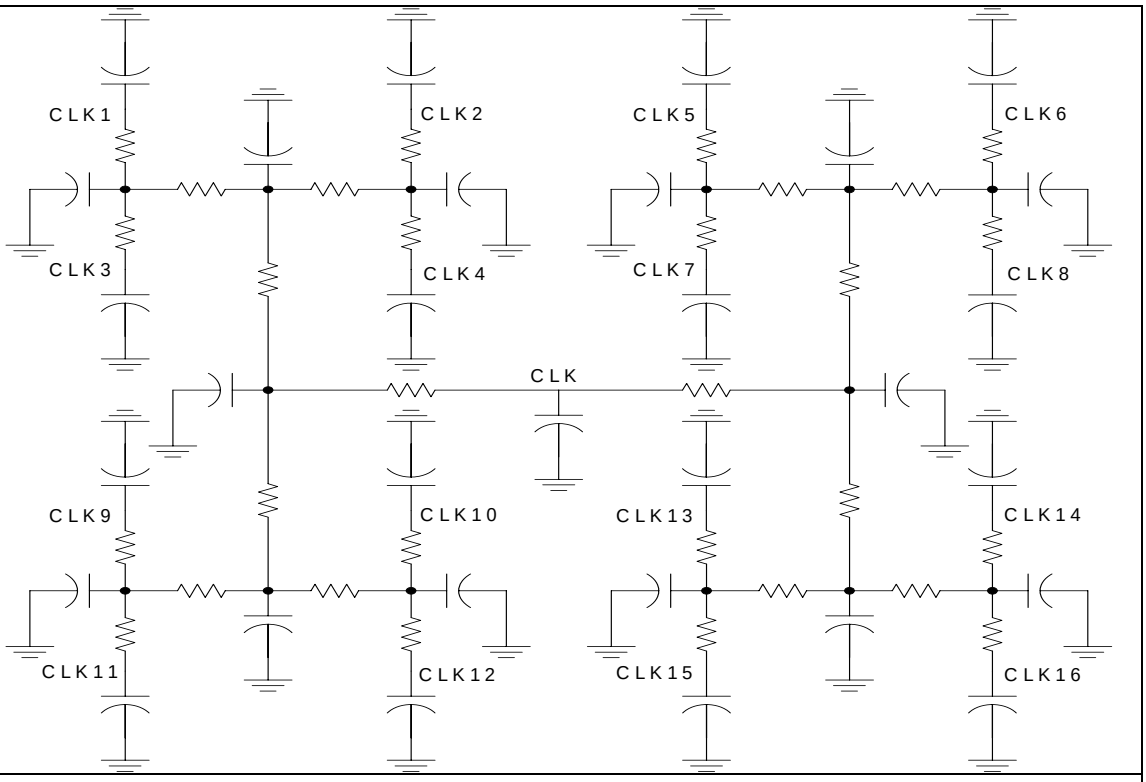

Fig 2: Distributed RC model of clock tree

2.1. Impact of PVT variations on ER clock

The Energy Recovery (ER) clock generator shown in Fig. 1(a) is vulnerable to Process Voltage-Temperature (PVT) variations. The amplitude of the waveform would change with changes in temperature and process parameters because of the resulting change in resistances in the oscillation path. Such amplitude variation is not acceptable as it could result in flip-flop malfunction or timing uncertainties. The PVT sensitivity can be reduced by introducing a pull-up transistor (M2) as shown in Fig. 3. Transistor M2 pulls up the clock signal to the full supply (Vdd), preventing variations in the oscillation amplitude. The pull up transistor M2 receives a pulse which has the same frequency but is out of phase with the pulse of the pull down transistor by 180 degrees. The pull up transistor is activated when the waveform reaches its peak, and hence pulling up or clipping the waveform to the full supply amplitude. Therefore, the clock generator is not affected by changes in temperature or threshold voltage. The pull up transistor is a fairly large transistor and is responsible for making the clock generator robust to process and temperature variations. Sensitivity to the main supply voltage (V_{dd}) variations cannot be reduced by M2; however, it does reduce the sensitivity of the oscillation amplitude to the $V_{dd}/2$ supply voltage variations. Fig. 4 shows a typical waveform generated by the energy recovery clock.

We simulated the clock generator at different temperatures and threshold voltages and measured the power consumed by the clock generator for the worst case scenario of the

amplitude degradation (temperature of 100 degrees Celsius and high threshold voltage corner). The power dissipated by the clock generator under the worst case scenario is 4.26 mW at 160 Mhz. Addition of the PMOS pull up comes at the cost of 85% increase in power dissipation of the oscillator.

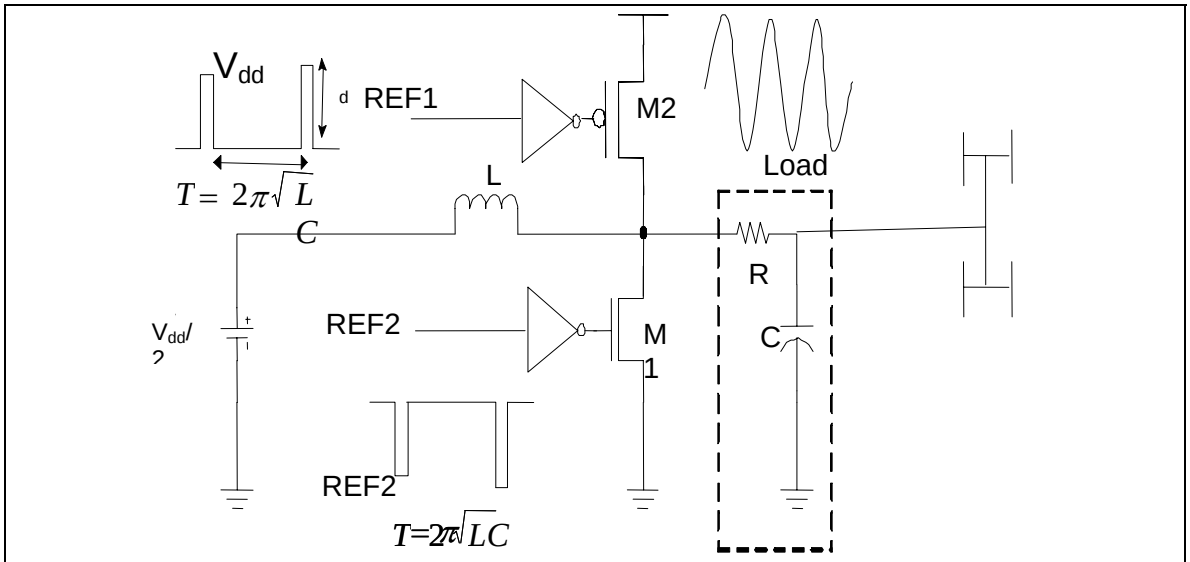

Fig 3: Energy recovery clock generator

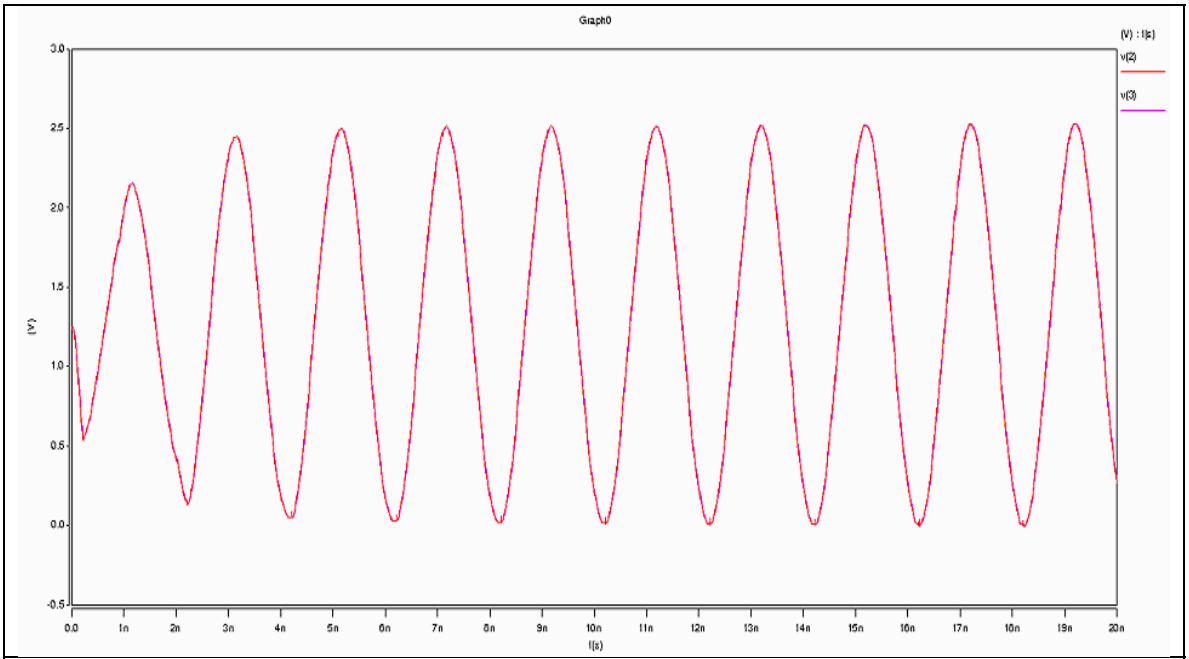

Fig 4: Typical waveform generated by the energy recovery clock generator

2.2. Oscillator Clock Gating

The clock generally has idle states during which it can be turned off else it would continue to run and consume the same amount of power as in the active state. We develop a clock gating technique for the oscillator to reduce the power consumed during the idle state. The proposed energy recovery clock generator with clock gating feature is shown in the Fig. 5.

The clock gating is implemented by replacing the inverters with the NAND gates that have the REF pulse and enable signal as their inputs. Moreover, a pass transistor switch is inserted in the half Vdd supply path to eliminate short circuit power in the clock gated mode when the pull down transistor is pulling the clock down to zero voltage. The pass transistor switch has to be a strong switch to reduce its associated loss of oscillator power efficiency. When the clock generator is active the enable signal is high and the switch is ON and when the clock generator is in an idle state the enable is low which would turn OFF the switch and the pull-up PMOS (M2) and turn ON the pull-down NMOS (M1). Hence, in the clock gated mode, the clock is gated to zero voltage and there is no switching happening at the gate of M1 and M2 transistors. This results in a substantial power saving in the oscillator.

Fig. 6 shows a typical waveform of the energy recovery clock generator with clock gating. The waveform shows that the clock generator is in the active state for the first few

cycles and then enters an idle state where the clock is gated to zero voltage. The oscillator is then enabled and it starts oscillating. Notice that the oscillator can generate a proper full amplitude clock waveform right after being enabled and there is no settling down time needed for activation. This is because of having the pull-up transistor. The power consumed by the clock generator during the active state is 14.8 mW which is considerably larger than the power of the original oscillator without clock gating (4.26 mW) (Fig. 3). This overhead is due to the addition of the NAND gates and the transmission gate switch which needs to be very large to efficiently implement the clock gating. This large overhead however can be offset by the power saved in idle sate. The power consumed during the idle state is 4.8 μW which corresponds to 1000 times reduction. This substantial power saving in the idle state can offset the clock gating power overhead if the system has sufficient probability of being in the idle state.

In order to compare the original and clock-gated energy recovery clock generators, we compare the power dissipation of each oscillator at different probabilities of idle sate (shown in Fig. 7). The power of the original oscillator is constant and independent of the probability of the sleep mode. The power of the clock gated oscillator reduces as the probability of the sleep mode increases. This analysis shows the sleep mode probability required for the clock gating to make sense to be applied to the oscillator. It is observed that a sleep mode probability of 72% or above is required for the oscillator clock gating to show overall power reduction. For any system with less than 72% of sleep mode, the

original clock generator is a better choice. Hence, the selection of clock generators is dependent on the sleep mode probability in any given system.

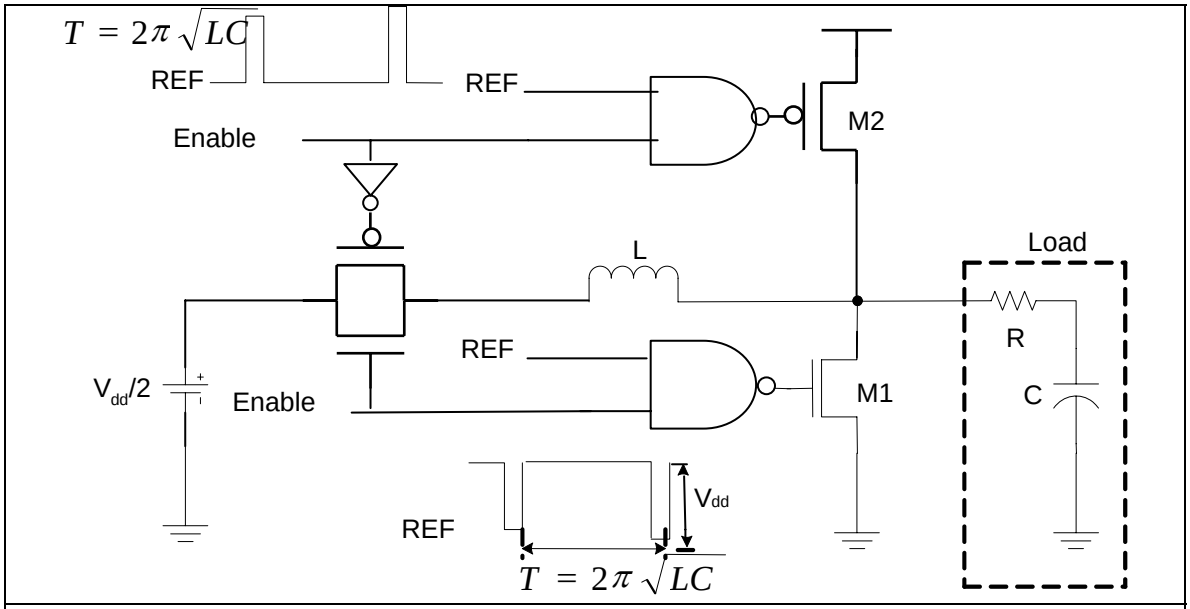

Fig 5: Energy recovery clock generator with clock gating

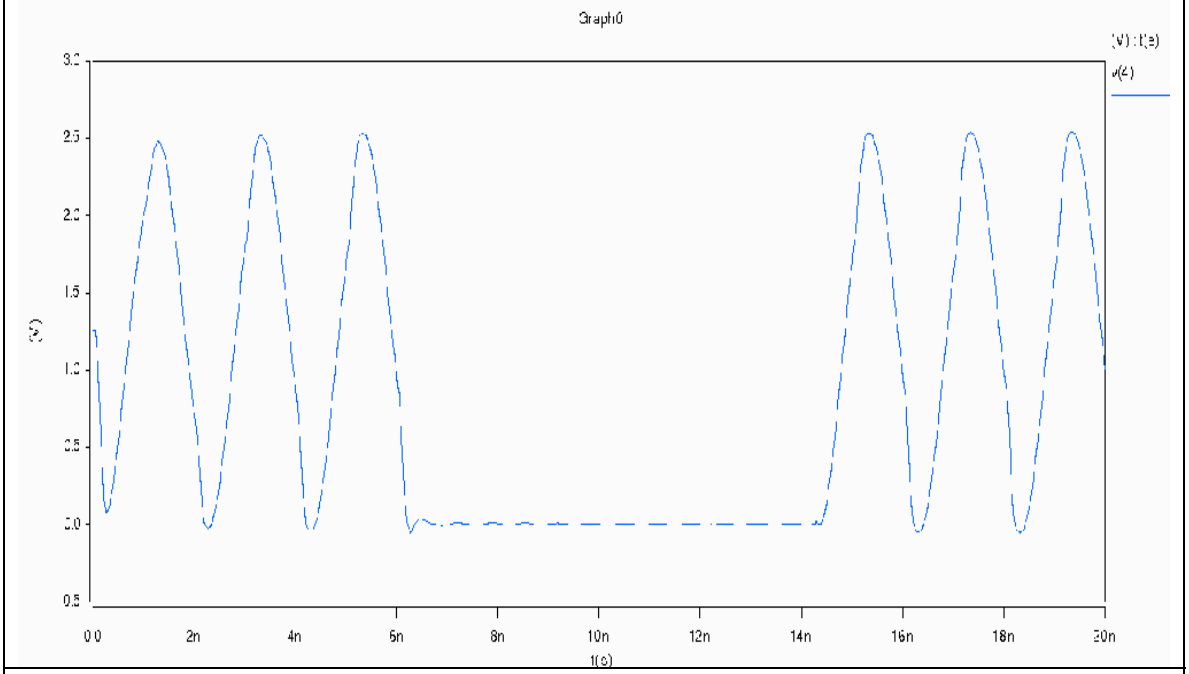

Fig 6: Typical waveform of the energy recovery clock with clock gating

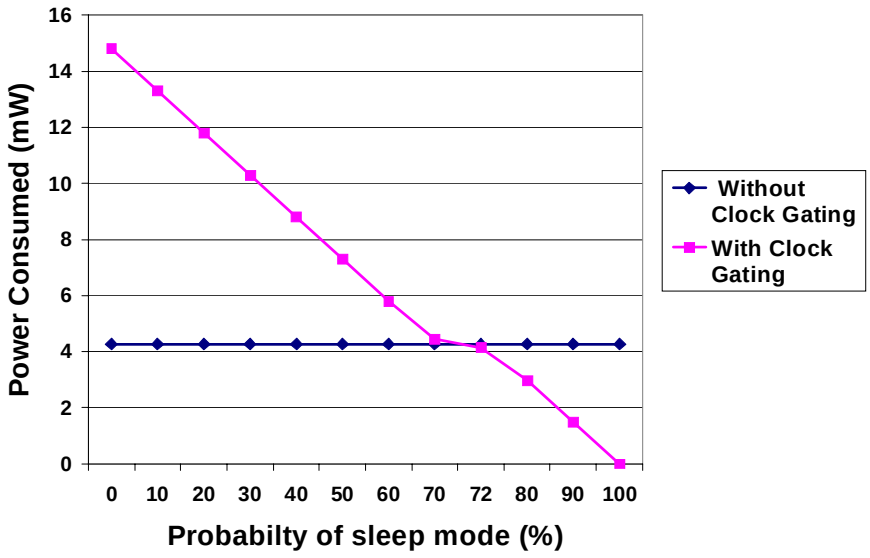

Fig 7: Comparison of energy recovery clock generators

3. Energy Recovery Flip Flops with Clock Gating

In this section, our proposed flip-flops, as well as the conventional energy recovery clocked flip-flop, are presented and their operations are discussed. Fig. 8 shows the schematic of a conventional Four-Phase Transmission-Gate (FPTG) energy recovery clocked flip-flop [3]. FPTG is similar to the conventional Transmission-Gate Flip-Flop (TGFF) [4] except that it uses 4-transisor pass-gates designed to conduct during a short fraction of the clock period. The energy recovery clock is a four-phase sinusoidal clock (CLK0, CLK1, CLK2, and CLK3). FPTG is a master-slave flip-flop with the master controlled by CLK0 and CLK2 and the slave controlled by CLK1 and CLK3. The main disadvantage of this flip-flop is its long delay. The delay from D to Q ($t_{D\text{-}Q}$) takes roughly half the effective clock period (T_{eff}). In addition, transistors required for the pass-gates are large, resulting in large flip-flop area.

Another approach for energy recovery clocked flip-flops is to locally generate square-wave clocks form a sinusoidal clock [3]. This technique has the advantage that existing square-wave flip-flops could be used with the energy recovery clock. However, extra energy is required in order to generate and possibly buffer the local square waves. Moreover, energy is not recovered from gate capacitances associated with clock inputs of flip-flops.

Recovering energy from internal nodes of flip-flops in a quasi-adiabatic fashion would also be desirable. However, storage elements of flip-flops cannot be energy recovering

because we assume that they drive standard (non-adiabatic) logic. Due to slow rising/falling transitions of energy recovery signals, applying energy recovery techniques to internal nodes driving the storage elements can result in considerable short-circuit power within the storage element. Taking these factors into consideration, we developed flip-flops that enable energy recovery from their clock input capacitance, while internal nodes and storage elements are powered by regular (constant) supply. Employing our flip-flops in system designs enables energy recovery from clock distribution networks and clock input capacitances of flip-flops.

Energy recovery clocking substantially reduces the clock power compared to the square wave clocking. However, there is still some power dissipated in the oscillator itself, on the clock network resistances, and inside the flip-flops. This clock power is a wasted power if the system is in the idle mode. We target further reducing the clock power in idle periods by the application of the clock gating technique to the energy recovery clock. Clock gating is a well known idea that is applied to square wave clock systems to reduce power in idle states [10]. In this section, we propose techniques for applying clock gating to the energy recovery clocking system in order to obtain additional power savings in the idle mode. All the results presented in this paper are obtained in a 0.25um CMOS technology with the supply voltage of 2.5V and at room temperature.

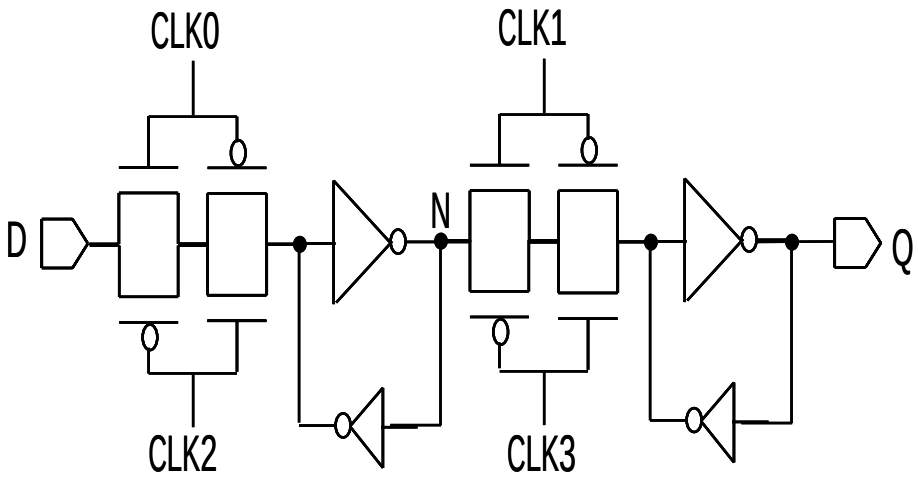

Fig 8: Conventional Four-Phase Transmission-Gate (FPTG) energy recovery clocked flip-flop [3]

3.1. SCCER

Fig. 9 shows a Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flip. The transistor MN3, controlled by the output QB, provides conditional capturing. The right hand side evaluation path is static and does not require conditional capturing. Placing MN3 above MN4 in the stack reduces the charge sharing. That is because when the charge sharing occurs, the capacitance associated with MN3 is already charged and therefore does not contribute to the charge sharing [12].

The flip flop dissipates the same amount of power during sleep mode and the active mode. A major portion of the power is dissipated by the clock network. We separated the clock network from the rest of the circuit and used a separate supply V(clk) for the clock network and measured the power dissipated by the clock network . Table 1 shows us the power dissipated by the clock network (P[clk]) and the rest of the flip-flop (P[vdd]) for different switching activities. Table 2 shows us the delay results for SCCER. We can save power by disabling the clock network during the sleep mode as significant amount of power is consumed by the clock network. We can disable the clock network by implementing clock gating.

Fig. 10 shows SCCER with clock gating. Clock gating was implemented by replacing the inverter with the NOR gate. The NOR gate has two inputs: the clock signal and the enable signal. In the active mode, the enable signal is low so the NOR gate behaves just

like an inverter and the flip-flop operates just like the original flip-flop. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. This turns off the pull down path (MN2) and prevents any evaluation of the data. Hence, not only the internal clock is stopped (clock power saving) but also all the internal switching is prevented (power saving on data circuits). Typical waveforms for SCCER flip-flop with clock gating are shown in the Fig. 11. The skewed inverter was replaced by a NOR gate. It should be mentioned that the skew direction for the NOR gate should remain as that in the original inverter gate (skewed for high to low transition; pull-down network stronger than pull-up).

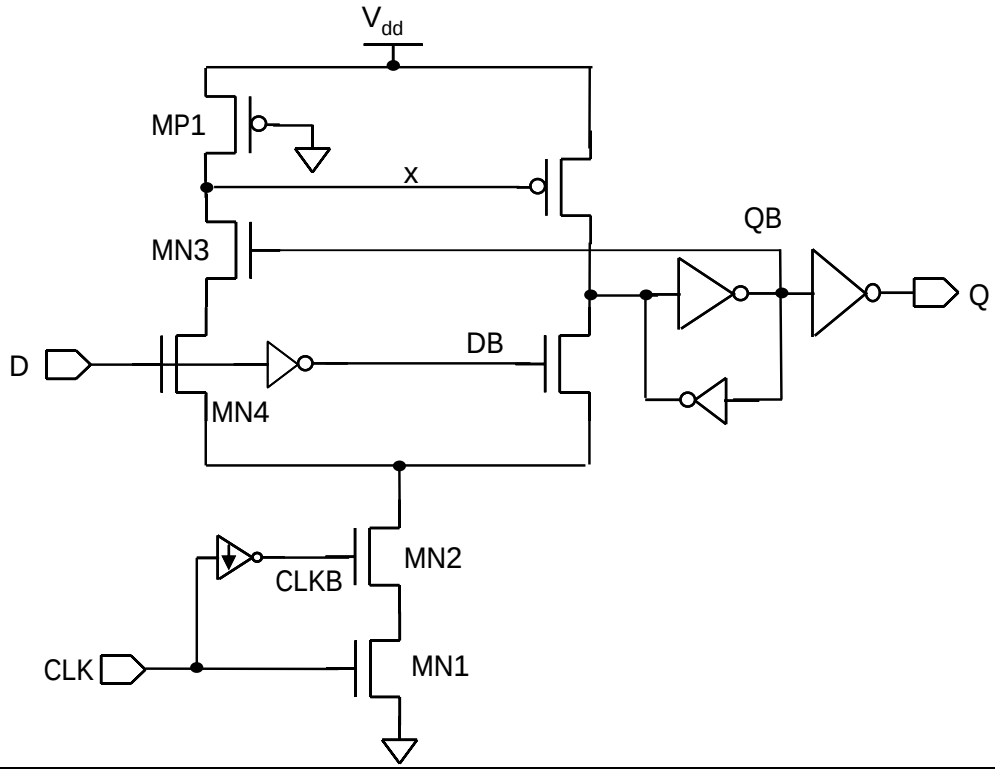

Fig 9: Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	4.5 n	12.3	12.3
50	45.5	11.1	56.6
100	99.6	9.0	108.6

Table 1: Power Results for SCCER

Set up time	40 ps
Hold time	60 ps
Clk-Q delay	232 ps
D – Q delay	277 ps

Table 2: Delay Results for SCCER

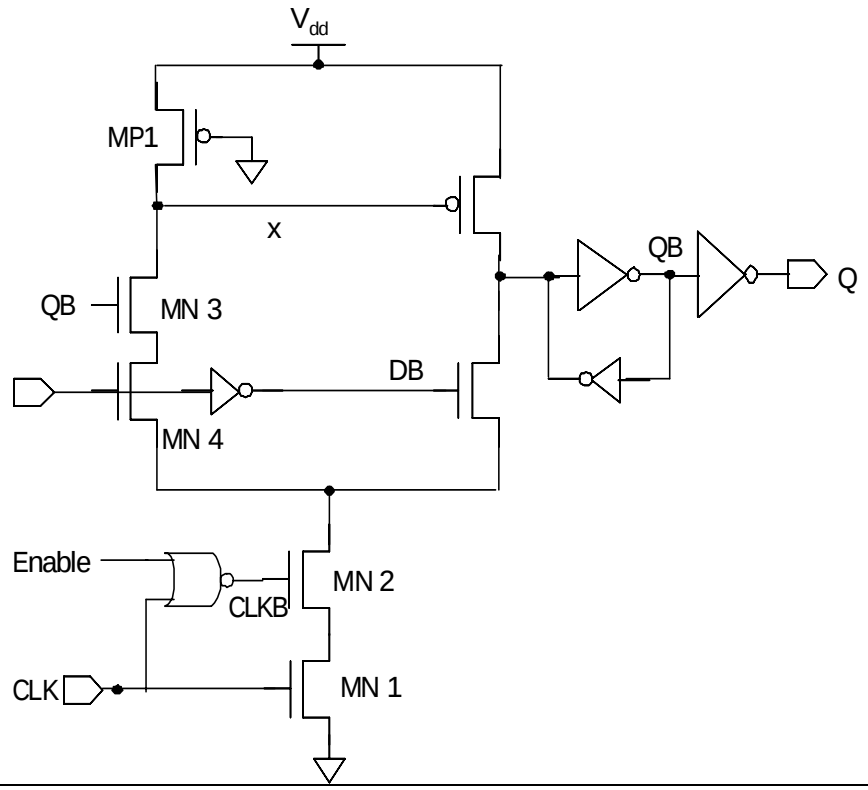

Fig 10: Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop with clock gating

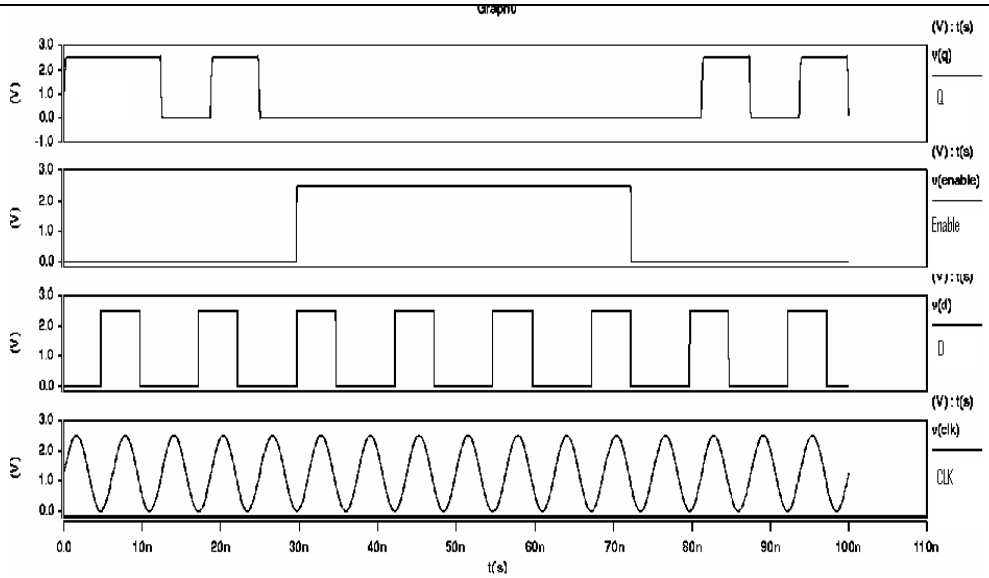

Fig 11: Typical waveforms for SCCER flip-flop with clock gating

Table 3 shows the power dissipated by SCCER during the active mode for different switching activities. Table 4 shows the power dissipated when clock gating is applied during the sleep mode for different switching activities. Results show that power savings of more than 1000 times are made due to clock gating. Table 5 shows us the delay results.

Table 6 shows us the overhead due to implementation of clock gating; there is no power overhead for implementing clock gating and a negligible delay penalty. We do not have power overhead as we use minimum sized transistors for the NOR gate and also reduction in the short circuit power dissipated on the logic gates connected to the sinusoidal clock (the NOR gate shows less short circuit power than the inverter gate due to larger stack of transistors). Our results show that we save 99.9% of power with clock gating during idle states when compared to the flip flop without clock gating. SCCER with clock gating shows power savings without any probability of sleep mode. Further savings are possible if there is some probability of sleep mode. Therefore, SCCER with clock gating is a better flip flop than the original SCCER without clock gating.

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	1.6 n	12.2	12.2
50	45.1	11.1	56.2
100	98.9	9.1	108

Table 3: Power results for SCCER during the active mode

Switching Activity (%)	P(vdd) (nW)	P(clk) (nW)	Total Power (nW)
0	6.7	3.2	9.9
50	5.7	3.0	8.7
100	13.1	3.0	16.1

Table 4: Power results for SCCER with clock gating during sleep mode

Set up time	40 ps
Hold time	60 ps
Clk-Q delay	237 ps
D – Q delay	282 ps

Table 5: Delay results for SCCER with clock gating

	SCCER (Overhead %)
Power	-0.7
Delay (clk-q)	2
Set up	None
Hold	None

Table 6: Overhead for SCCER with clock gating for 50% data switching activity

3.2. DCCER

Fig. 12 shows the Differential Conditional-Capturing Energy Recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a precharge and evaluate fashion. However, instead of using the clock for precharging, small pull-up PMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based Set/Reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output (Q and QB) to the control transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data (D and DB) is same as that of the output (Q and QB), both left and right evaluation paths are turned off preventing SET and RESET from being discharged. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle [12].

Due to its sinusoidal nature, the CLK signal is generally less than Vdd/2 during a significant part of the conducting window. Therefore, a fairly large transistor is used for MN1. Moreover, since there are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become ON simultaneously. Having properly sized pull-up PMOS transistors (MP1 and MP2) instead of clock controlled precharge transistors ensures a constant path to V_{dd}, which helps to reduce the effect of charge sharing. Although MP1 And MP2 are statically ON, they do not result in static power dissipation because as soon as the data sampling finishes and Q obtains the values

of D, the pull down paths get turned off and the SET and RESET nodes are pulled back high without any static power being dissipated. Another property of the circuit that helps reduce charge sharing is that the clock transistor (MN1), which is the largest transistor in the evaluation path, is placed at the bottom of the stack. Therefore, the diffusion capacitance of the source terminal of MN1 is grounded and does not contribute to the charge sharing [12]. The power results for DCCER are obtained in a similar way as the SCCER. Table 7 shows the power and Table 8 shows delay results.

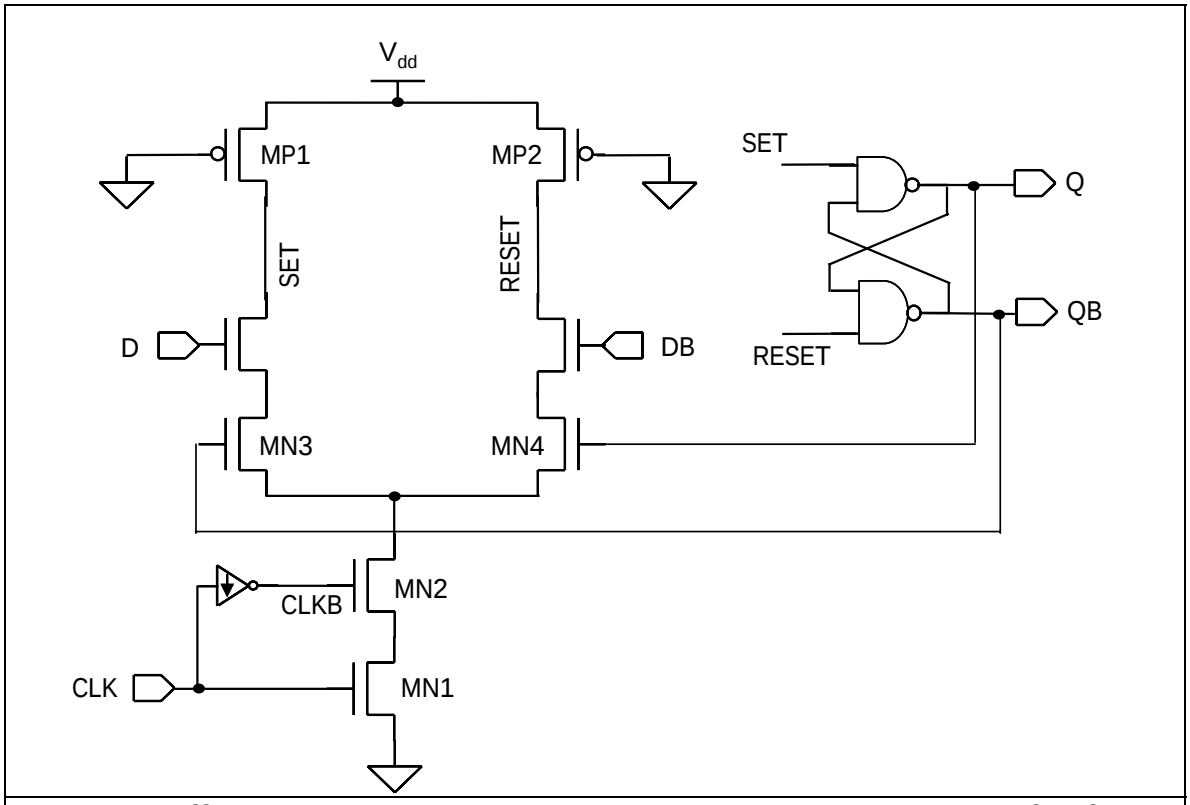

Fig 12: Differential Conditional Capturing Energy Recovery (DCCER) flip-flop

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	11.8 n	12.4	12.41
50	51.0	11.0	62.0
100	106.7	9.4	116.1

Table 7: Power Results for DCCER

Set up time	140 ps
Hold time	130 ps
Clk-Q delay	184 ps
D – Q delay	329 ps

Table 8: Delay Results for DCCER

Figure 13 shows the DCCER with clock gating. Clock gating in DCCER in was implemented in the same manner as it was implemented in the SCCER. When DCCER is in sleep mode, enable becomes low which disables the clock network and reduces power significantly. Our results power savings of 99.9% because of clock gating. Table 9 shows the power dissipated by DCCER during the active mode for different switching activities. Table 10 shows the power dissipated when clock gating is applied during the sleep mode for different switching activities. Results show that power savings of more than 1000 times are made due to clock gating. Table 11 shows us the delay results. Table 12 shows us the overhead due to implementation of clock gating; there is negligible power overhead for implementing clock gating and a considerably less delay penalty.

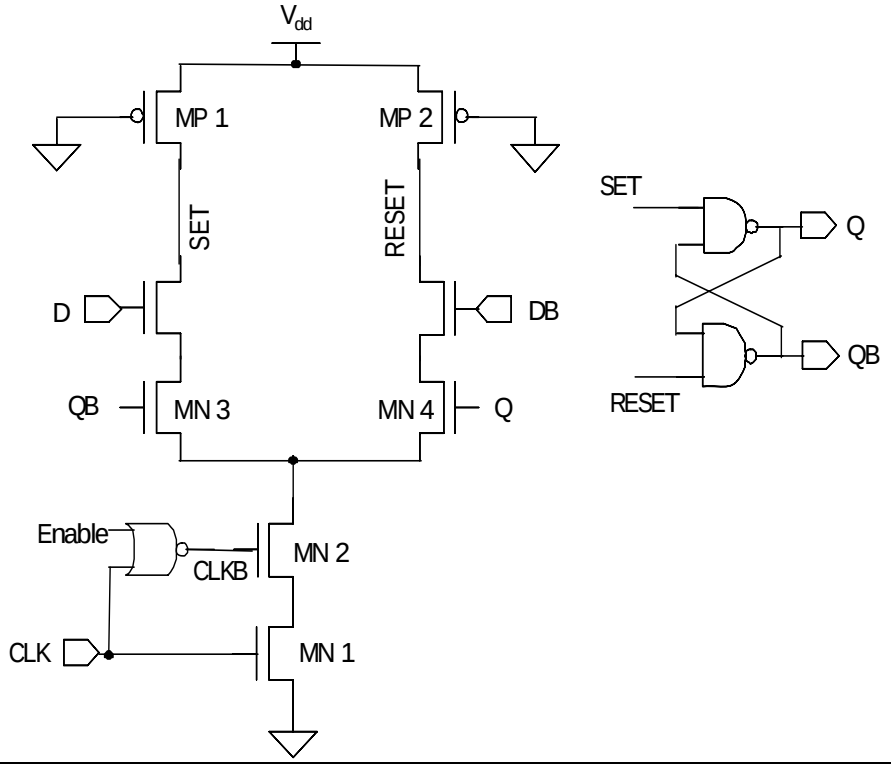

Fig 13: Differential Conditional Capturing Energy Recovery (DCCER) flip-flop with clock gating

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	10 n	12.1	12.11
50	51.4	10.8	62.2
100	107.4	9.4	126.8

Table 9: Power results for DCCER during the active mode

Switching Activity (%)	P(vdd) (nW)	P(clk) (nW)	Total Power (nW)
0	0.33	3.01	3.34
50	1.1	3.2	4.3
100	1.0	3.1	4.1

Table 10: Power results for DCCER with clock gating during sleep mode

Set up time	140 ps
Hold time	130 ps
Clk-Q delay	205 ps
D – Q delay	350 ps

Table 11: Delay results for DCCER with clock gating

	DCCER (Overhead %)
Power	0.3
Delay (clk-q)	11.4
Set up	None
Hold	None

Table 12: Overhead for DCCER with clock gating for 50% data switching activity

3.3. SDER

Fig. 14 shows the Static Differential Energy Recovery (SDER) flip-flop. This flip-flop is a static pulsed flip-flop similar to the Dual-rail Static Edge-Triggered Latch (DSETL) [7]. The energy recovery clock is applied to a minimum-sized inverter skewed for fast high-to-low transition. The clock signal and the inverter output (CLKB) are applied to transistors MN1 and MN2 (MN3 and MN4). The series combination of these transistors conducts for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltages above the threshold voltages of the NMOS transistors. Since the clock inverter is skewed for fast high-to-low transitions, the conducting period occurs only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB). However, due to the slow rising nature of the energy recovery clock, enough delay can be generated by a single inverter. In this flip-flop, when the state of the input data is the same as its state in the previous conduction phase, there are no internal transitions. Therefore, power consumption is minimized for low data switching activities. The second approach for minimizing flip-flop power at low data switching activities is to use conditional capturing to eliminate redundant internal transitions [12]. Table 13 shows power results measured similarly as the previous flip flops.

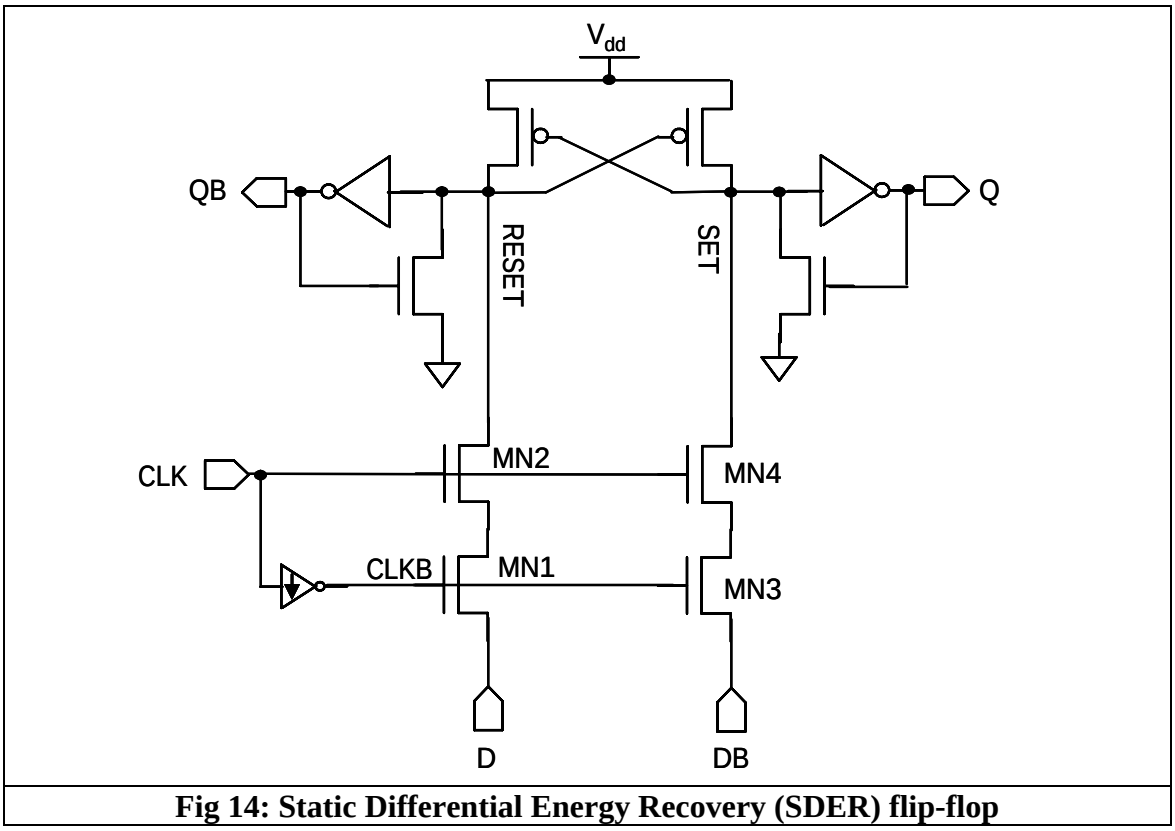

Fig 14: Static Differential Energy Recovery (SDER) flip-flop

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	3.2 n	19.7	19.7
50	62.7	19.8	82.5
100	126	20.0	146

Table 13: Power Results for SDER

Set up time	150 ps
Hold time	140 ps
Clk-Q delay	185 ps
D – Q delay	330 ps

Table 14: Delay Results for SDER

Figure 15 shows the SDER with clock gating where the skewed inverter was replaced by a NOR gate. The technique used is similar to the one used for previous flip flops. Power results show significant savings when the clock gating is applied to the flip flop during the idle state. Power savings of more than 1000 times are made during the idle sate when compared to the power consumed to without clock gating. Table 15 shows the power dissipated by SDER during the active mode for different switching activities. Table 16 shows the power dissipated when clock gating is applied during the sleep mode for different switching activities. Results show that power savings of more than 1000 times are made due to clock gating. Table 17 shows us the delay results. Table 18 shows us the overhead due to implementation of clock gating; there is no power overhead for implementing clock gating and a considerably less delay penalty.

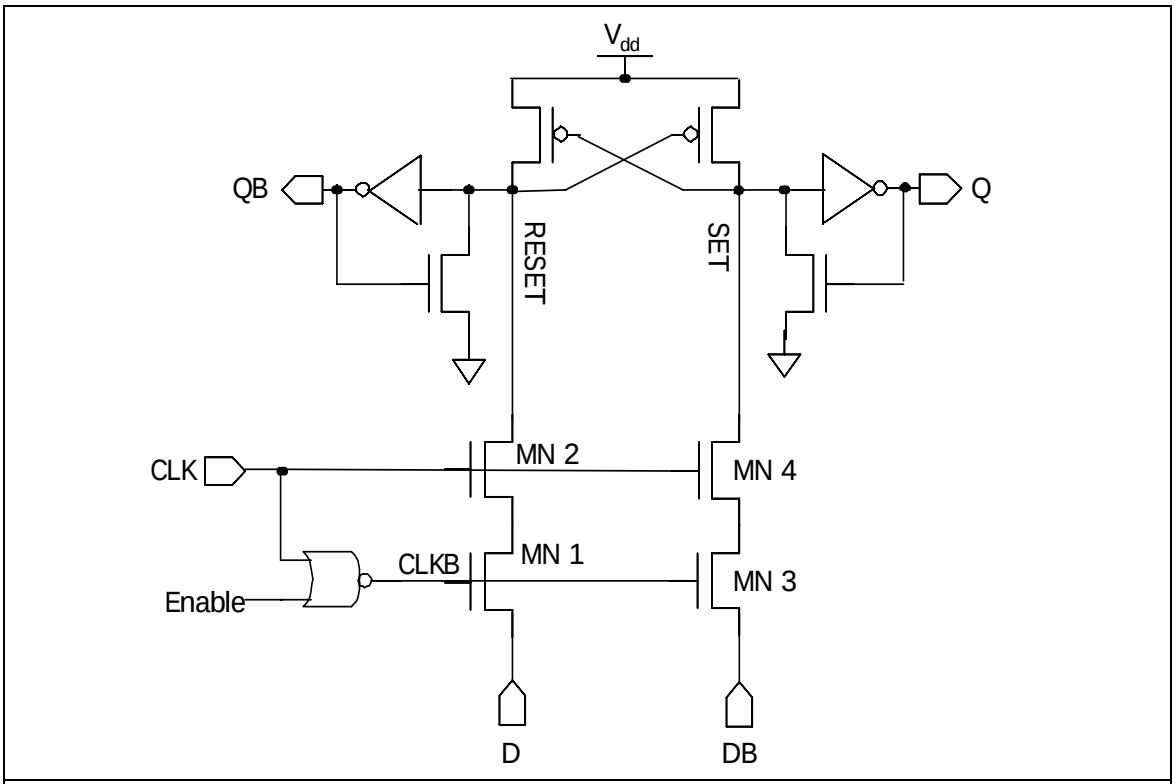

Fig 15: Static Differential Energy Recovery (SDER) flip-flop with Clock Gating

Switching Activity (%)	P(vdd) (µW)	P(clk) (µW)	Total Power (µW)
0	22.5 n	18.8	18.82
50	63.5	18.9	82.4
100	127.7	19.0	136.7

Table 15: Power results for SDER during the active mode

Switching Activity (%)	P(vdd) (nW)	P(clk) (nW)	Total Power (nW)
0	11.5	3.1	14.6
50	11.6	2.84	14.44
100	10.1	2.92	13.02

Table 16: Power results for SDER with clock gating during sleep mode

Set up time	140 ps
Hold time	130 ps
Clk-Q delay	202 ps
D – Q delay	347 ps

Table 17: Delay results for SDER with clock gating

	SDER (Overhead %)
Power	-0.1
Delay (clk-q)	9.1
Set up	None
Hold	None

Table 18: Overhead for SDER with clock gating for 50% data switching activity

4. Summary of Results

Table 19 shows results for the power consumed during the active mode for 50% data switching activity in both the original and clock gated flip-flops. It is observed that the clock gating does not introduce any power overhead. This is because of the use of small transistors in the NOR gates and also reduction in the short circuit power dissipated on the logic gates connected to the sinusoidal clock (the NOR gate shows less short circuit power than the inverter gate due to larger stack of transistors).

Table 20 shows results for the power consumed during the sleep mode for 50% data switching activity. Power results show significant savings when the clock gating is applied to the flip-flop during the idle state. Power saving of more than 1000 times is obtained during the idle state when compared to the power consumed without clock gating. The power savings increase with increase in the data switching activity.

Table 21 shows the delay comparisons between the original flip-flops and the flip-flops with clock gating. The results show that the clock gating addition has no impact on setup and hold time of the flip-flops. The delay overhead is caused by an increase in the clock to output (clk-Q) delay due to addition of NOR gates. The overhead in the data to output (D-Q) delay is less than 6.3%.

Original flip-flops in Active Mode				Flip Flops with clock gating in Active Mode		
	Data power (µW)	**Clock power (µW)**	**Total Power (µW)**	**Data power (µW)**	**Clock power (µW)**	**Total Power (µW)**
SCCER	45.5	11.1	56.6	45.1 (-0.8%)	11.1 (0%)	56.2 (-0.7%)
DCCER	51.0	11.0	62.0	51.4 (0.7%)	10.8 (-1.8%)	62.2 (0.3%)
SDER	62.7	19.8	82.5	63.5 (1.2%)	18.9 (-4.5%)	82.4 (-0.1%)

Table 19: Comparison of power consumption during active mode for 50% data switching activity

(Numbers inside parentheses represent % overhead)

Original flip-flops in Sleep Mode				Flip Flops with clock gating in Sleep Mode		
	Data power (µW)	**Clock power (µW)**	**Total Power (µW)**	**Data power (nW)**	**Clock power (nW)**	**Total Power (nW)**
SCCER	45.5	11.1	56.6	5.7 (99.9)	3.0 (99.9)	8.7 (99.9)
DCCER	51.0	11.0	62.0	1.1 (99.9)	3.2 (99.9)	4.3 (99.9)
SDER	62.7	19.8	82.5	11.6 (99.9)	2.8 (99.9)	14.4 (99.9)

Table 20: Comparison of power consumption during sleep mode for 50% data switching activity

(Numbers inside parentheses represent % saving)

	Original flip-flops				Flip Flops with clock gating			
	Set up Time (pS)	**Hold Time (pS)**	**Clk – Q Delay (pS)**	**D-Q Delay (pS)**	**Set up Time (pS)**	**Hold Time (pS)**	**Clk – Q Delay (pS)**	**D-Q Delay (pS)**
SCCER	40	60	232	277	40	60	237	282 (1.8%)
DCCER	140	130	184	329	140	130	205	350 (6.3%)
SDER	150	140	185	330	150	140	202	347 (5.1%)

Table 21: Comparison of delay for 50% data switching activity

(Numbers inside parentheses represent % overhead)

5. Negative Edge Triggering

The existing energy recovery clocked flip-flops are positive edge triggered. In a synchronous system, there is a need for both positive and negative edge triggered flip-flops. Unlike square wave clocked flip-flops, it is not possible to have negative edge triggering by simply inverting the clock signal. This is because inversion of a sinusoidal clock signals using an inverter gate destroys the signal and eliminates its energy recovery property. Hence, negative edge triggering requires a separate design for flip-flops. The existing flip-flop designs can be modified to obtain negative edge triggering as shown in Fig. 16, 17 and 18. Fig. 16 shows the negative edge triggered version of SCCER. The negative edge triggered SCCER is a complement of the positive edge triggered SCCER. Similarly the negative edge version of DCCER and SDER are devised by complementing their positive edge triggered design as shown in Fig. 17 and 18.

Table 22 shows the power and delay results obtained for the negative edge triggered flip-flops and their comparison with the positive edge triggered flip-flops. There is a considerable power overhead due to increase in number of PMOS transistors in the negative edge triggered flip-flops and also due to the larger sized PMOS transistors needed to obtain functional negative edge triggered flip-flops. There is no delay penalty for the negative edge triggered SCCER which ensures the same performance as the positive edge triggered SCCER. Negative edge triggered SDER has power savings compared to the positive edge triggered SDER. Negative edge DCCER performance is very similar to that of the positive edge triggered DCCER.

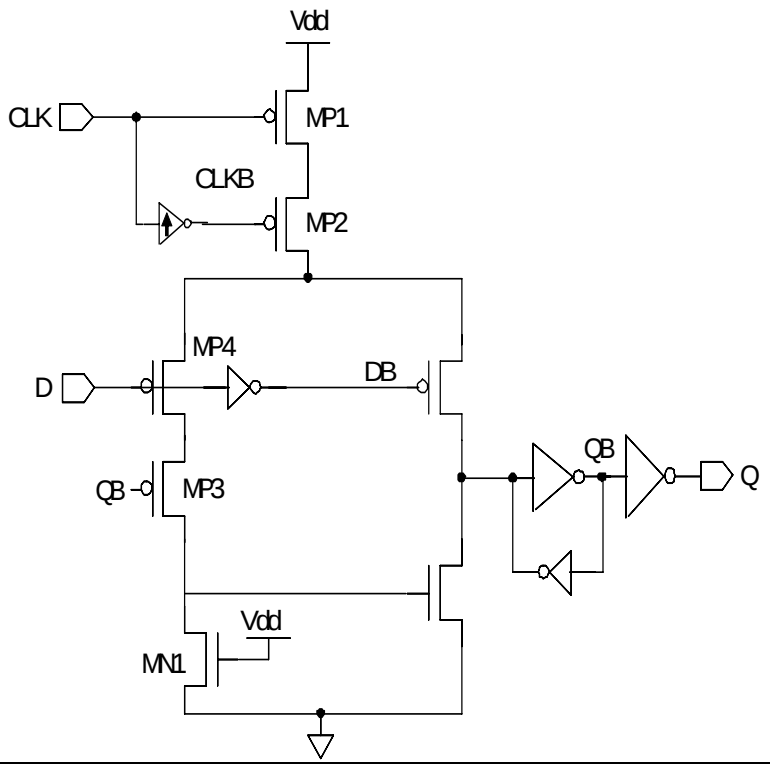

Fig 16: Negative Edge Single-ended Conditional Capturing Energy Recovery (SCCER)

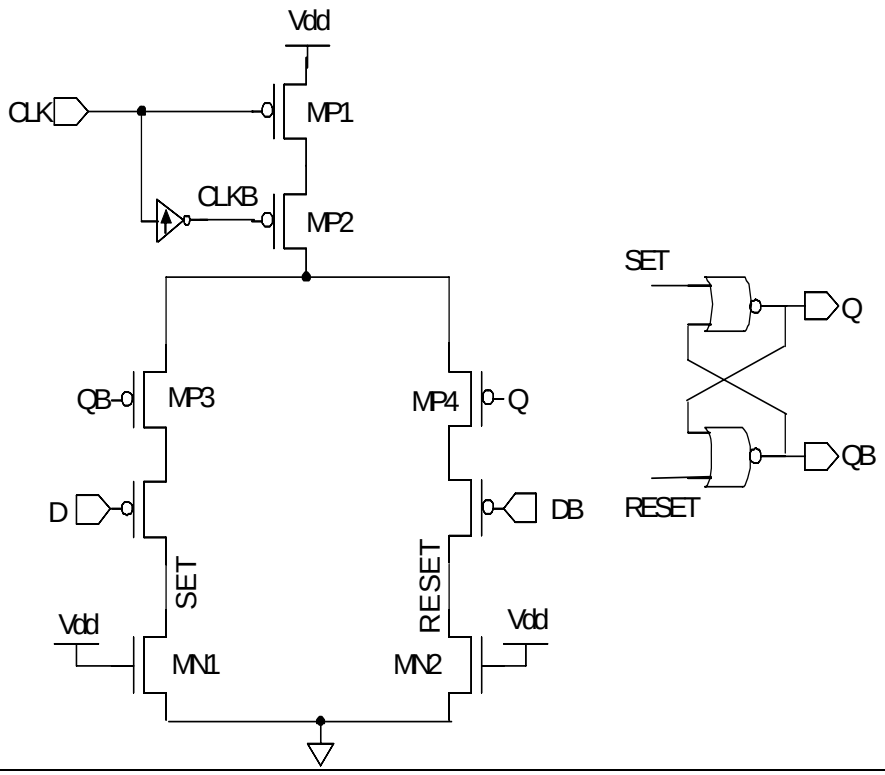

Fig 17: Negative Edge Differential Conditional Capturing Energy Recovery (DCCER) flip-flop

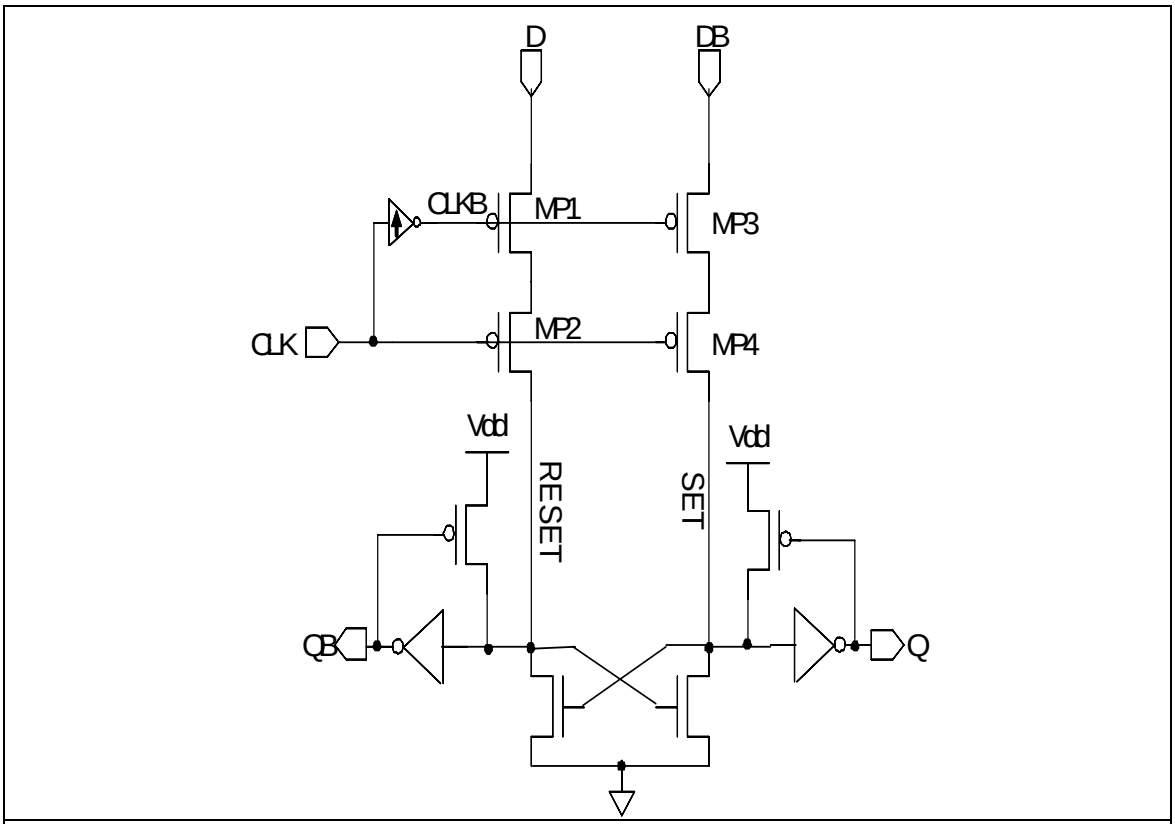

Fig 18: Negative Edge Static Differential Energy Recovery (SDER) flip-flop

	SCCER		DCCER		SDER	
	Positive Edge	**Negative Edge**	**Positive Edge**	**Negative Edge**	**Positive Edge**	**Negative Edge**
Power (µW)	56.6	109 (92%)	62.1	133 (114%)	82.5	81.8 (-0.8%)
Delay (clk-q) (pS)	232	194 (-16%)	184	208 (13%)	185	593 (220%)
Set up time (pS)	40	70	140	170	150	120
Hold time (pS)	60	130	130	430	140	280

Table 22: Comparison of negative and positive edge flip-flops at 50% switching activity

(Numbers inside parentheses represent % overhead)

6. Comparison of Clock Gating Approaches

As explained before, there are two approaches for clock gating at the system level. One approach is to use a clock gated oscillator and stop the main clock. In this case, the flip-flops do not need to be clock gated since the clock is gated to zero. The second approach is to use an original oscillator but apply the clock gating to the flip-flops. In this section, we provide a comparison between these two clock gating approaches.

To do this comparison, we integrated 1000 SCCER flip-flops through an H-tree clock network driven by the clock generator. There are three design cases: design 1 consists of an energy recovery clock generator without clock gating driving 1000 integrated SCCER positive edge triggered flip-flops without clock gating; design 2 consists of an energy recovery clock generator with clock gating driving 1000 integrated SCCER positive edge triggered flip-flops without clock gating; ; design 3 consists of an energy recovery clock generator without clock gating driving 1000 integrated SCCER positive edge triggered flip-flops with clock gating. We have compared total power dissipation in these approaches for different data switching activities and different probabilities of sleep mode (Fig. 9).

Fig. 19, 20 and 21 show the comparison of the three design approaches for the data switching activity of 0%, 50%, and 100%, respectively. The plots show the total system power vs. the sleep mode probability. It is observed that for applications with sleep mode probability greater than 72% (regardless of data switching activity) design approach # 2 (oscillator clock gating) is the best choice. For sleep mode probabilities less than 72%

(regardless of data switching activity), design approach # 3 (flip-flop clock gating) is the best choice as it consumes less power compared to the other cases. Therefore, the choice of the clock gating approach is dependent on the probability of the sleep mode for any given application. For a sleep mode probability of 50% and data switching activity of 50%, the flip-flop clock gating technique reduces the system power by 47%.

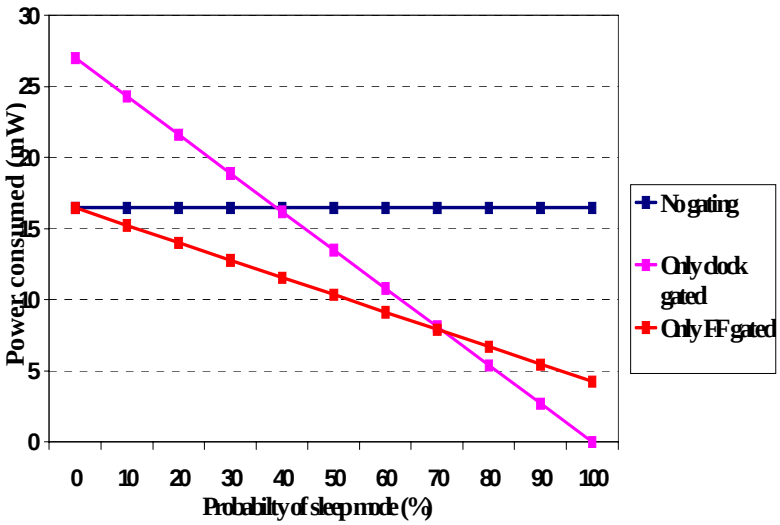

Fig 19: 0% data switching activity

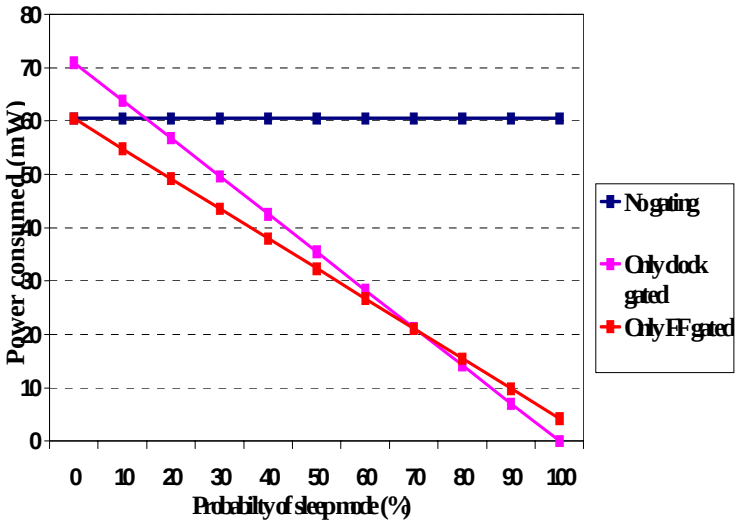

Fig 20: 50% data switching activity

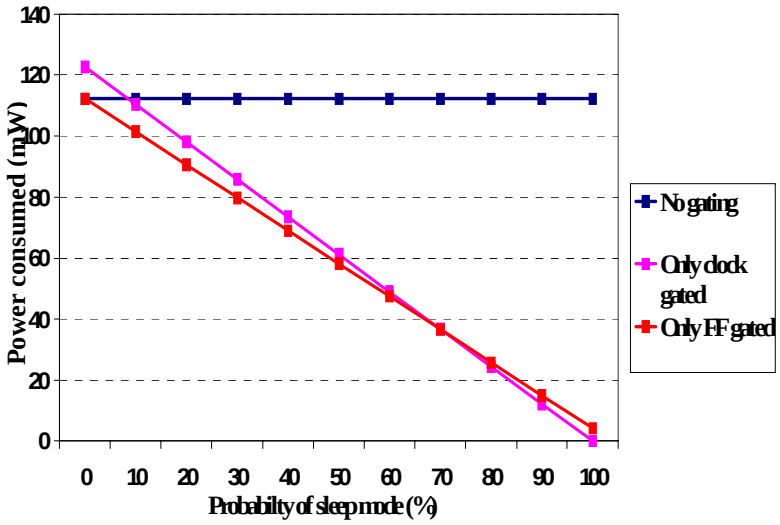

Fig 21: 100% data switching activity

7. Conclusion

We applied clock gating to the energy recovery clock generator and also to three energy recovery clocked flip-flops. Clock gating in energy recovery clocked flip-flops result in significant power savings during the idle state of the flip-flops without any considerable overhead compared to the original flip-flops. We then compared different clock gating approaches by integrating 1000 energy recovery clocked flip-flops and a clock generator. It is observed that for applications with very high sleep mode probability (above 72%) oscillator clock gating is the most power optimal clock gating solution and for applications with lower idle state probabilities, flip-flop clock gating is the most power optimal clock gating approach. Applying the proposed clock gating technique to the system of 1000 flip-flops with idle mode probability and data switching activity of 50%, reduces the total power by 47%. We also designed negative edge triggered energy recovery clocked flip-flops. Negative edge triggered flip-flops provide flexibility in designing an energy recovery system by having both positive and negative edge triggering options. Due to their considerable overheads compared to positive edge triggered flip-flops, negative edge triggered flip-flops should be used only when they are absolutely required. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption.

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